



LXT9785

Frequently Asked Questions

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As of January 15, 2001, this document replaces the Level One document *LXT9785 FAQs*.



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1.0 Questions and Answers

1.1 Introduction

This document is a composite of the most frequently asked questions (FAQs) and corresponding answers for the LXT9785, Intel's lowest power, highest performance octal transceiver.

1.2 Key Features

Q1. What are the key features of the LXT9785?

The following items are key features of the device:

- Low power, 2.5V operation.
- 10BASE-T and 100BASE-TX over UTP cabling.
- 100BASE-FX Fiber Optic capability.
- Multiple RMII, SMII, or SS-SMII interfaces for independent PHY port operation.
- Supports both auto-negotiation and legacy link partners that do not have auto-negotiation capability.
- Configurable via MDIO port or external control pins.
- Auto-MDIX crossover.
- "Sectionalization" allows this device to be used as two individual 4-port PHYs or a single 8-port PHY.
- Available in both 208-pin PQFP and 241-ball BGA packages.
- CDE protection greater than 5000V.
- Designed for superior EMI performance.
- JTAG boundary scan.
- Robust baseline wander correction.

1.3 Interface Modes

Q2. What is the Reduced Media Independent Interface (RMII)?

The LXT9785 provides a Reduced Media Independent Interface (RMII) for each network port, passing received data to the MAC: $RXD_{n<1:0>}$, $RXER_n$, and CRS_DV_n (where n reflects the port's number). Three signals are used to transmit data from the MAC: $TXD_{n_<1:0>}$ and $TXEN_n$. Both receive and transmit signals are clocked by REFCLK. Data transmission across the RMII is implemented in di-bit pairs, which is equal to a 4-bit-wide nibble.

This interface requires a single 50 MHz reference clock for both transmit and receive signals.

Q3. What is the Serial Media Independent Interface (SMII)?

The Serial Media Independent Interface (SMII) satisfies the following requirements:

- The SMII interface provides further pin/trace reduction over the RMII interface.
- Conveys complete MII information between a 10/100 Mbps PHY and MAC with two pins per port.
- Allows for a multi-port MAC/PHY communication with one system clock.
- Operates in both half-duplex and full-duplex.
- Performs per-packet switching between 10 Mbps and 100 Mbps data rates.
- Allows direct MAC-to-MAC communication.

All SMII ports use a common 125 MHz reference clock and SYNC signals that are synchronous to the reference clock. There are two signals in SMII from MAC-to-PHY for each port (TXD and TxSYNC), and one signal per port from PHY-to-MAC (RXD).

Q4. What is the Source Synchronous-Serial Media Independent Interface (SS-SMII)?

A new revision to the SMII Specification 2.1 defined a new Source Synchronous-Serial Media Independent Interface (SS-SMII). SS-SMII allows for a longer trace length and helps to relieve timing constraints, requiring the addition of four new signals, (TX_CLK, TX_SYNC, RX_CLK, and RX_SYNC). The transmit TX_CLK and TX_SYNC are sourced from the MAC to the PHY and referenced to the REFCLK input. The receive RX_CLK and RX_SYNC are sourced by the PHY to the MAC in reference to the REFCLK.

All SMII applications that use these additional signals are referred to as Source Synchronous.

Q5. What is the importance of the boundary scan (JTAG) function on the LXT9785?

The boundary scan (JTAG) function allows electrical access to every pin on the LXT9785, allowing boundary-level testing where signals can be driven out and input pins can be sensed via control from a 5-pin interface (TRST, TCK, TMS, TDO, and TDI). This may cause a reduction in the number of test points needed, resulting in a simplified board and lower costs.

1.4 Sectionalization

Q6. What is the LXT9785 Sectionalization concept?

The LXT9785's sectionalization function allows easier design with MACs and ASICs that do not have a multiple of eight ports. The Section pin allows the device to be configured into a single 8-port, or two independent 4-port sections, each with its own MDIO interface and MDC clock.

1.5 Initialization

Q7. What is the Power-Down Mode on the LXT9785?

The LXT9785 incorporates numerous features to maintain the lowest power possible. The device can be put into a low-power state via register 0.11, as well as a near-zero power state with the power-down pin. When the device is in the power-down mode, it cannot transmit or receive packets. *For more information, please refer to the Operating Requirements Section in the LXT9785 data sheet.*

1.6 General Information

Q8. What is Auto-MDIX?

The LXT9785's Automatic MDI Crossover (Auto-MDIX) feature detects the position of the link partner's transmit and receive cable pairs and determines whether they are aligned correctly. If not, it automatically swaps the transmit and receive signals internally, eliminating the need for installation of a crossover cable when connecting peer-to-peer. *For more information about the Auto-MDIX feature or its use, please refer to Application Note 122 (MDIX functional overview) on the Intel website.*

Q9. What are the magnetic requirements for the LXT9785?

The LXT9785 requires a 1:1 ratio transformer for both the receive and transmit transformer twisted-pairs. The device uses a current-driven driver (to save power) and requires both magnetic center taps to be connected together to analog VCC. *See Application Note 151, Design and Layout Guide for the LXT9785, for more information on design and recommended transformers.*

Q10. Why is no termination required for the LXT9785?

The load termination resistors for the TX and RX pairs of the LXT9785 are integrated into the device. This technique helps reduce the analog power of the PHY and reduces total system cost by eliminating 16 resistors per device.

Q11. What is the significance of the LXT9785 Next Page feature?

The Next Page feature allows the LXT9785 to share additional information with its link partner during auto-negotiation. Next Page exchange occurs only if both ends of the link advertise their ability to exchange Next Pages.

Q12. What are the targeted markets for the LXT9785?

The LXT9785 is appropriate in many designs. However, it is designed especially for stand-alone, stackable, and modular 10/100 Ethernet switches and routers.

Q13. Are BSDL and IBIS model files available for the LXT9785?

Both Boundary Scan Description Language (BSDL) files and I/O Buffer Information Specification (IBIS) models for the LXT9785 are available through the Intel website (<http://developer.intel.com/design/network/>).

Q14. What collateral is available for the LXT9785 on the Intel website (<http://developer.intel.com/design/network/>)?

The LXT9785 collateral listed below may be found on the Intel website (<http://developer.intel.com/design/network/>):

- Data Sheet
- Product Brief
- Design and Layout Guide (AN-151)
- Migration Guide: LXT9781/LXT9782 to LXT9785 (AN-152)
- Four demo board user guides (SS-SMII, SS-SMII (Fiber), SMII, and RMII)

Q15. Are LXT9785 reference designs or evaluation tools available?

The following fully functional evaluation boards and their documents are available for the LXT9785 device:

- SS-SMII PQFP Demo Board
- SMII PQFP Demo Board
- SS-SMII PQFP Fiber Demo Board
- RMII PQFP Demo Board
- RMII BGA Demo Board

Schematics for all of the demo boards are included in the user guides. System reference designs for the LXT9785, including Intel Media Switch devices as well as designs with other vendors' switches, are available. CAD files, UNH test reports, and information on system reference designs may be obtained from your local Intel representative.

Q16. What temperature options are available in the LXT9785?

The LXT9785 is available in a commercial temperature range only. If extended operating conditions are required, the LXT9784 is available with this option.

Q17. What is the availability of samples and production quantities?

Samples of the LXT9785 are now available and production is in progress. The lead-time for production quantities is dependent on volume ordered.